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The Operational Characteristics and Potential Applications of a Low Voltage EMCCD in a CMOS Process

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ABSTRACT

The Electron Multiplying Test Chip 1 (EMTC1) was developed with the aim of creating a device which could produce superior Electron Multiplication (EM) gain at a greatly reduced voltage. An EM gain exceeding 3% per stage has been recorded for a relatively low voltage (~13.0V) from two recently developed pixel structures. An electro-optical characterisation of the EMTC1 is presented focusing on charge transfer via experimental and simulation results aiming to provide insight into the transfer and multiplication process. The Charge Transfer Inefficiency (CTI) is analysed with the aim of providing a greater understanding of the charge transfer process. Light starved applications such as Earth observation and automated inspection are known to benefit from Time Delay Integration (TDI) and electron multiplication. Though traditionally implemented in CCDs, implementing TDI in CMOS technology can lead to an increase of functionality, higher readout speeds and reduced noise. This paper presents a discussion of the implication of these results on the potential applications of this sensor.

Keywords: EMCCD, CMOS image sensors, CTI, charge transfer

1. INTRODUCTION

The demand for imaging technology capable of achieving high readout speeds for low light environments has continued to grow. It is possible for traditional Charge Coupled Devices (CCDs) to achieve readout noise equivalent to several electrons [1] providing high sensitivity; however, this is only possible at relatively slow readout speeds. The Electron Multiplying Charge Coupled Device (EMCCD) was developed to overcome this limitation and allow for single photon detection at video rates. This is possible due to an additional multiplication register which enables on-chip gain, increasing the signal packet size above the readout noise. The additional gain register contains an array of elements designed to produce an area of high electric field through which the signal packet passes.

The traditional EMCCD is a 4-phase device that is clocked much like a CCD to transfer charge through the device (Figure 1). Two gates are clocked with normal amplitude drive pulses (P1 and P3). An additional gate (DC gate) is placed prior to phase 2 (P2) and is held at a constant voltage. Phase 2 is pulsed at a higher amplitude and is described as the high voltage gate. The potential difference between these two gates, which creates a region of high field accelerates the electrons to energies sufficient to achieve impact ionisation, generating electron-hole pairs from interactions with the silicon lattice. Additional charge is liberated and leads to an increase in the signal packet. The DC gate (P2DC) acts as a barrier and while the high voltage gate (P2HV) is clocked high. If the device is operated with low clocked amplitudes on P2HV, the EM gain is unity and the EM gain stage operates just like a normal CCD element.

By altering the biases of the gates, it is possible to transfer the charge packet from one stage to the next where the process of impact ionisation is repeated until readout is reached. The multiplication gain per stage is small, typically 1-1.5%, however, many stages are implemented (>500) and it is possible to achieve gain upwards of several thousand [2]. These devices often require the P2HV voltage to be within the range of 40-50 V to produce such gain.

EMCCDs have found multiple uses within a range of fields from biomedical [3] to astronomical [4] imaging. However, limitations such as the required high P2HV voltage can be problematic when implementing a sensor in a ‘power restricted’ environment.

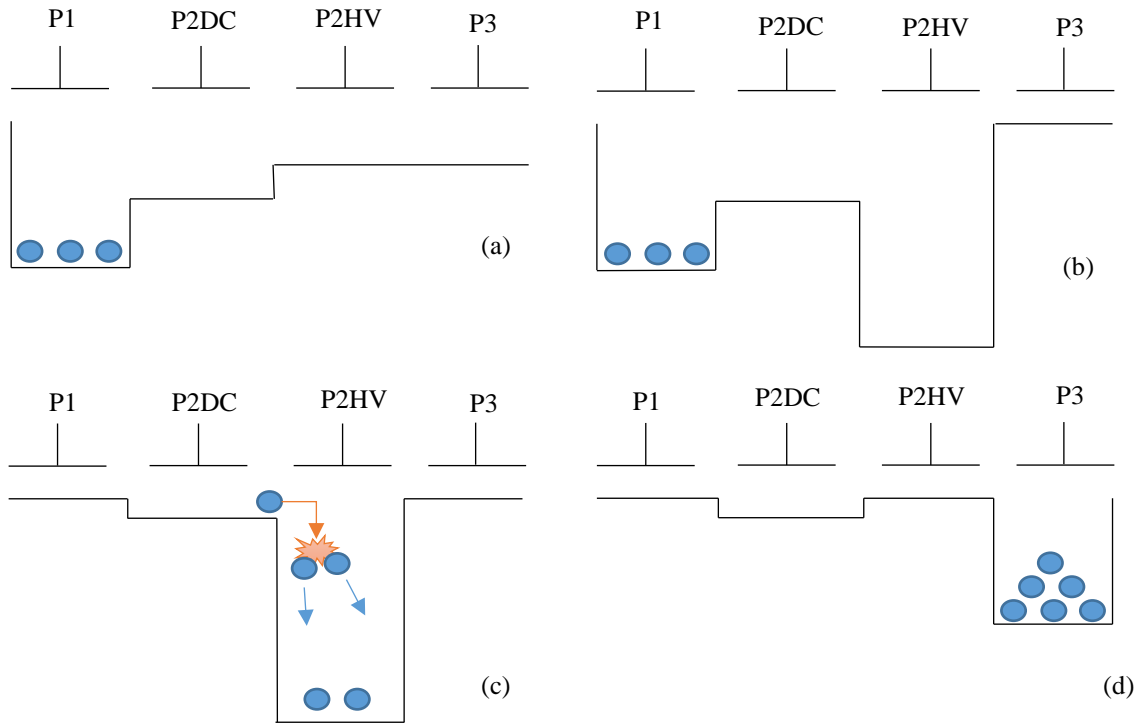


Figure 1: An example of EMCCD clocking. The charge is initially held under the P1 gate (a). A region of high field is established (b). Impact ionisation occurs as the charge is transferred between P2DC and P2HV (c), before the signal is then moved out to the next multiplication element (d).

CMOS (Complementary Metal-Oxide Semiconductor) sensors have become the norm in consumer, and more recently in professional cameras. Lately, there has also been a rise in the number of CMOS image sensors deployed in spacecraft [5]. The higher radiation tolerance and reduced power consumption [6] of CMOS imagers compared to CCDs make them well suited for astronomical imaging. However, there have been limited studies into the implementation of electron multiplication in CMOS image sensors [7, 8] due to difficulties arising from the lack of overlapping gates.

2. CHARGE TRANSFER EFFICIENCY

Within a CCD or an EMCCD image sensor, light is detected via the photoelectric effect. An incident photon leads to the generation of an electron-hole pair, and the electron is collected within a potential well beneath a gate in the buried channel. The size of the charge packet within the potential well directly correlates to the light intensity incident on one pixel. The charge can be easily transferred between potential wells by altering the biasing of the gates, moving the signal packet to the next potential well, eventually enabling the image to be read out. It is essential to minimise any charge losses during this transfer process due to the large number of transfers that each charge packet must undergo before image readout. The ability to perform this process is characterised by the Charge Transfer Efficiency (CTE), which is defined the fraction of charge that is successfully transferred. It is also possible to describe the converse characteristic, the Charge Transfer Inefficiency (CTI), where $CTI = 1 - CTE$.

For modern CCDs the CTI is around 10^{-5} [9]. The CTI depends on the charge packet size and a number of other factors including bulk and surface damage due to irradiation. This is relevant when considering EMCCDs device, which experience an additional damage process called ageing [10]. This process demonstrates as a decrease in the EM gain over the operating period of the device and has been attributed to charge trapping beneath the DC gate [11]. Traps are known to play a pivotal role in increasing the CTI, and there has been considerable interest in the nature of traps formed by radiation damage and subsequent effect on the charge transfer efficiency [12]. Studies into the ageing process have also provided insight into the development of traps during the operation of EMCCDs and the subsequent effect on the CTI [10].

3. THE ELECTRON MULTIPLYING TEST CHIP 1

The Electron Multiplying Test Chip 1 (EMTC1) was developed to provide electron multiplying capability in a CMOS process. The device has demonstrated gain exceeding 3% per stage at 293 K, achieved at a third of the voltage required by commercial devices, ~ 13 V. Manufactured by the ESPROS corporation [13], the device implements two novel EM elements with the aim of substantially increasing the gain at lower voltages than those in traditional EMCCDs. The device is subdivided into eight blocks of 32 columns, with each block containing a different pixel structure. The first two blocks operate as a normal 4-phase CCD to provide a reference. Blocks 3-6 contain EMCCD pixels with rectangular HV gate but each differing in width and length, the sizes of which can be found in Table 1. The final blocks 7-8 contain the two new pixel structures. Further information pertaining to the structure of these pixels will be provided in a future paper.

Table 1: Table denoting each pixels shape and size for the EMTC1. The first two blocks provide a CCD reference.

Block number	Pixel Parameters		
	HV gate type	HV gate length (μm)	HV gate width (μm)
Block 1	4-phase CCD (No EM)		
Block 2	4-phase CCD (No EM)		
Block 3	Rectangular	3.0	6.0
Block 4	Rectangular	2.5	6.0
Block 5	Rectangular	3.0	5.0
Block 6	Rectangular	2.5	5.0
Block 7	Staircase	2.5-3.5	5.0
Block 8	Spike	1.6-2.6	5.0

4. EMTC1 SIMULATION

Successful charge transfer can be challenging when implementing a CCD or EMCCD in a CMOS process as overlapping or closely spaced gates are not commonly available. This can lead to an incomplete transfer of charge and poor CTE. The CTE performance of sensors implemented in a CMOS process is still often worse than in modern CCDs [14].

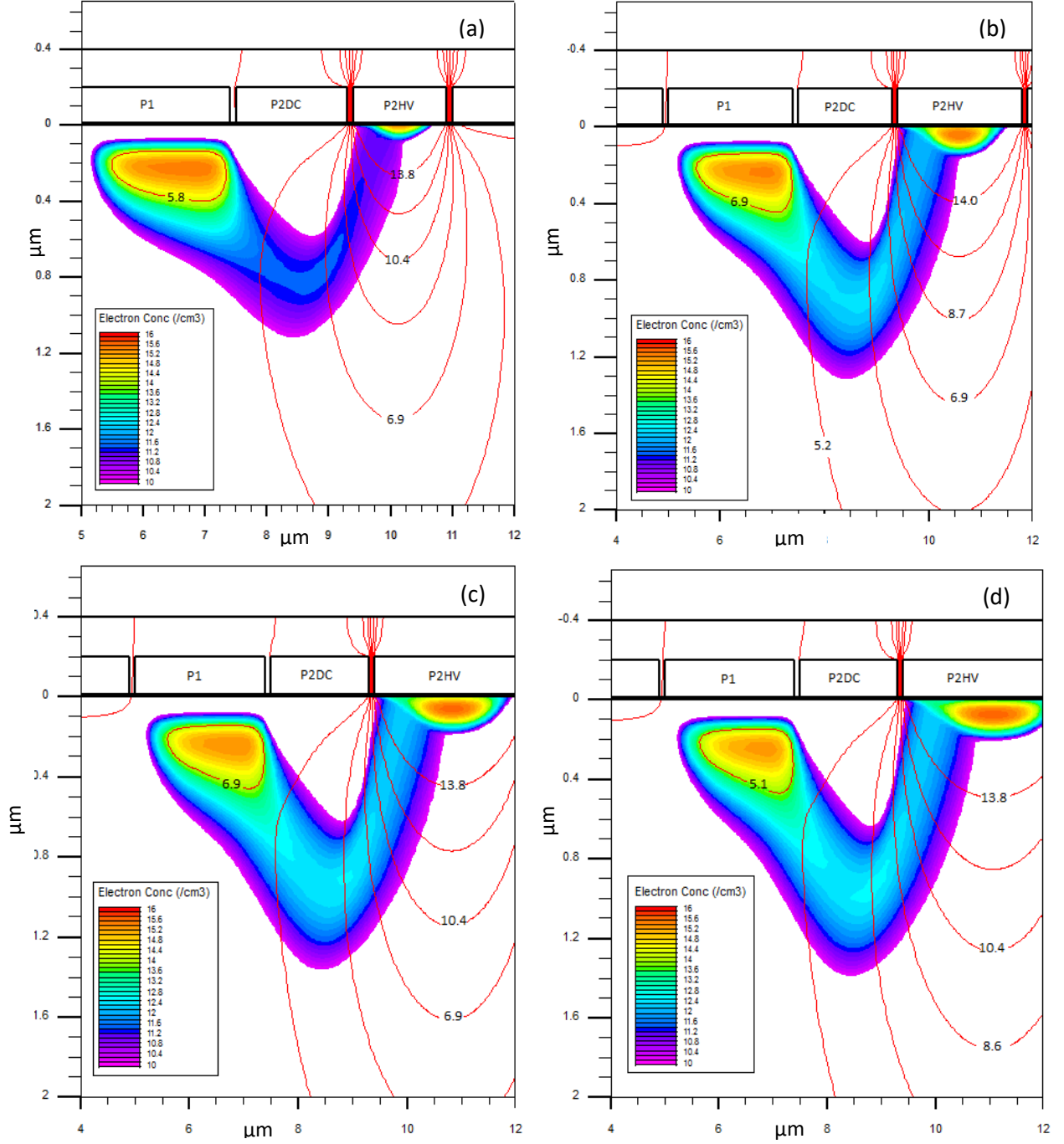


Figure 2: Electron concentration beneath the P2DC and P2HV gates at 293 K, 3 ns after the P1 began to decrease starting the charge transfer process to P2HV for gate lengths of 1.6 μm (a); 2.5 μm (b); 3.0 μm (c) and 3.5 μm (d). P2DC was biased at 3.0 V while P2HV was clocked at 15.0 V. The contours denote the potential in volts.

Atlas, a commercial software provided by Silvaco, was utilised to simulate the charge transfer in the EM pixel structures. This was completed in 2D with the device features chosen to model the EMTC1 as realistically as possible. Appropriate physical models were selected to replicate the internal physics of the EMTC1. These include implementing a mobility model based on one proposed by Lombardi [15] and an impact ionisation model based by Selberherr [16]. An input signal of approximately 1000 electrons was used to perform the transfer, and the device was clocked with timings consistent with running the EMTC1 under normal operating conditions. The device simulation enabled several device parameters to be quantified visually, including the carrier concentration and the regions where impact ionisation is most likely to occur.

The device simulation mirrored the device operation of a traditional EMCCD. The simulated device was illuminated and charge collected in a potential well for a set period. Once the charge had fully collected within the initially empty potential well, under P1, the charge was moved to P2HV which was already raised to a high voltage. It is between the P2DC and P2HV gates that a region of high field is located, as shown in Figure 1, and where the majority of impact ionisation occurs.

Figure 2 demonstrates the concentration of the electrons beneath the P2DC and P2HV and the location of charge beneath these gates taken at 3 ns after the start of the transfer from P1 to P2HV. While the charge is primarily located in the same region relative to P1 and P2HV, it can be noted that for the shortest gate length, Figure 2 (a), the charge cloud is much closer to the surface than for the longer gate lengths (Figure 2(b-d)). It is apparent that for smaller gate structures a smaller proportion of charge has been transferred during the same transfer time. As such the time for total charge transfer is decreased from ~13 ns for a gate length of 1.6 μm to ~0.5 ns for a gate length of 8 μm .

Figure 3 demonstrates the location in which the impact ionisation occurs when 50% of the charge has been transferred from beneath P1 to P2HV. The impact ionisation region extends deeper into the device beneath the gap between the P2DC and P2HV gate as the P2HV gate length increases. This can be attributed to the increased electric field which peaks at greater distances from the interface, subsequently the charge storage region moves deeper into the device.

It can be seen in Figure 3 that the regions of high-intensity impact ionisation extend towards the Si-SiO₂ interface of the device. If the electrons are accelerated to an energy greater than 3.6 eV near the Si-SiO₂ interface it is possible for a carrier to come into contact with the interface and the gate dielectric. It is this charge that can lead to the creation of traps and the subsequent increase in CTI. If this process is repeated multiple times, then it is possible for a build-up of these traps to occur and the gain of the device to reduce with each subsequent transfer. The buried channel in an EMCCD or CCD moves the charge storage region away from the Si-SiO₂ interface, reducing the interaction with surface traps. However, high gate potentials could lead to the charge density extending closer towards the interface. Figure 3 (a) demonstrates that for the shorter gate length the potential has a high value closer to the gate than that seen in the longer gates. Subsequently, the charge will be accelerated in a region closer to the interface, leading to a greater number of 'hot' charge carriers closer to the interface and an increased probability of traps generation.

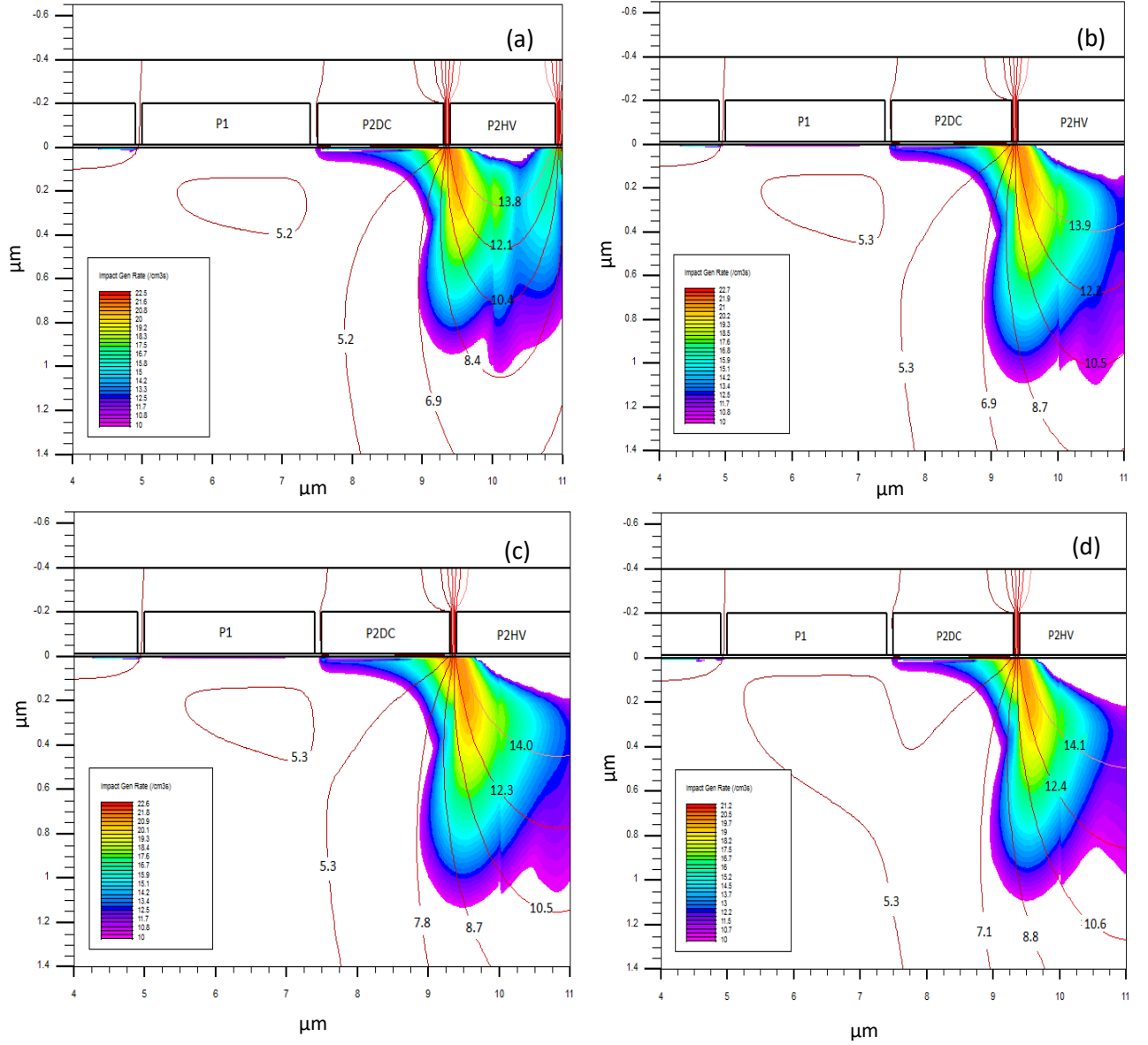


Figure 3: The regions of the impact ionisation beneath the P2DC and P2HV gates at 293 K. for gate lengths of 1.6 μm (a); 2.5 μm (b); 3.0 μm (c) and 3.5 μm (d) when 50% of the charge had been transferred from P1 to P2HV. P2DC was biased at 3.0 V while P2HV was clocked at 15.0 V. The contours denote the potential in volts.

The region of impact ionisation is primarily located beneath the gap between the P2DC and P2HV gates, however, it is of interest to note that a second smaller region of impact ionisation also exists directly beneath P2DC, extends towards the Si-SiO₂ interface. During impact ionisation, holes also experience acceleration. These holes are accelerated in the opposite direction to the electrons and are attracted to the least positive potential well within close vicinity, the P2DC gate.

If these holes have a threshold energy that exceeds 5.0 eV (a value higher than that of electrons), it is possible for them to have sufficient energy to interact with the interface states. It has been hypothesised that as trapped holes accumulate after each transfer [10] the potential of the P2DC gate decreases leading to a reduction in the gain per stage. It is of interest to note that the size and location of the impact ionisation region beneath the P2DC gate is largely uniform for all gates lengths implying that the location of charge is uniform beneath P2DC. As such it can be assumed that the quantity of charge trapped is constant across the devices and subsequently the EM ageing is uniform across the different pixel structures.

Due to the nature of the 2D simulation, it is difficult to adequately simulate a gate structure, as such, only the length has been taken into consideration here.

5. EXPERIMENTAL RESULTS

While the simulation data provides qualitative insight into the internal physical processes of a semiconductor image sensor, reliable quantitative simulation data can be harder to attain. As such, it was important to provide a comparison in the form of an electro-optical characterisation of the device. Previous papers [17] [18] have presented work comprising a study of the dark current, photoelectric response and the damage induced by proton irradiation and EM ageing of the EMTC1. These studies have provided insight into the effect of the biasing on the charge transfer process especially in relation to the effect on the EM gain.

Photon Transfer Curve

The Photon Transfer Curve (PTC) [19] provides a standardised test procedure which enables the measurement of the read noise, the full well capacity, the linearity and the conversion gain. The PTC is dependent on the assumption that if the flat illumination images have been differenced and the fixed pattern noise removed, the remaining noise consists only of read noise and shot noise. As the input signal increases the dominant noise source changes from read noise to shot noise. The device then experiences saturation and a drop in the PTC curve can be seen. The photon transfer curve can also be utilised to enable the analysis of several important device characteristics including the full well capacity and the read noise. Figure 4 demonstrates that temperature has no effect on the photon transfer curve while providing insight into the full well capacity and read noise which can be found in Table 2.

Table 2: Several EMTC1 characteristics obtained from mean-variance photon transfer curve at 293 K. These values have been collected by averaging over five devices. The full well capacity was acquired from the signal at 5% non-linearity.

	Operational Characteristics at 293 K
Full well Capacity (e-)	$\sim 116000 \pm 2000$
Read noise at 10 kHz line rate (e- RMS)	50 ± 4
Conversion Gain (e-/ADU)	12.2 ± 0.4

Table 2 provides the full well capacity, the readout noise and the conversion gain of the device. The full well capacity is comparable to many modern EMCCD devices [20] which have a similar or larger pixel size. Furthermore the read noise at 10 kHz line rate was acquired when operated without gain and was found to be considerably higher than in several CCDs [20-22].

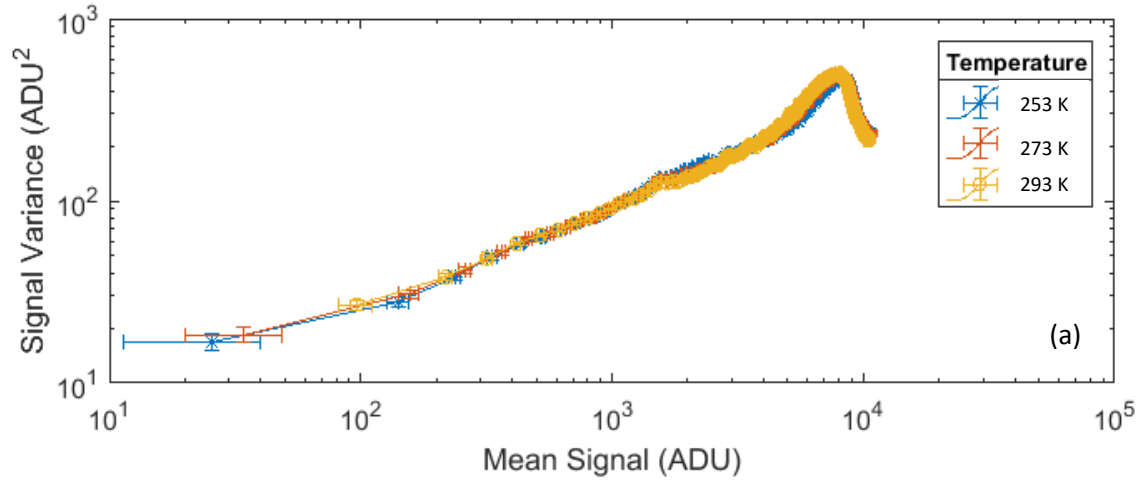


Figure 4: a) Mean-variance photon transfer curve for Block 5 at several temperatures. The device was operated without gain (P2HV)

Dark Current

Much like a CCD, cooling an EMCCD leads to a reduction in the dark current. This reduction is significant when considering that the dark signal noise acts as a contributing factor to the system noise which is then multiplied at the same time as the desired photon-generated signal. This cooling can lead to an increase in spurious charge which occurs when secondary charge is produced even when no primary charge is present. This charge is typically considered as part of the total dark current.

The dark current has been measured for a number of EMTC1 sensors and the average dark current for each region of interest has been calculated. Figure 5 shows Arrhenius plots of the pixel dark current for several EMTC1 sensors. It can be observed that the dark-current values decreases with temperature and within the temperature range the curve exhibits two regions. This non-uniformity between the dark current can largely be contributed to the test nature of the device.

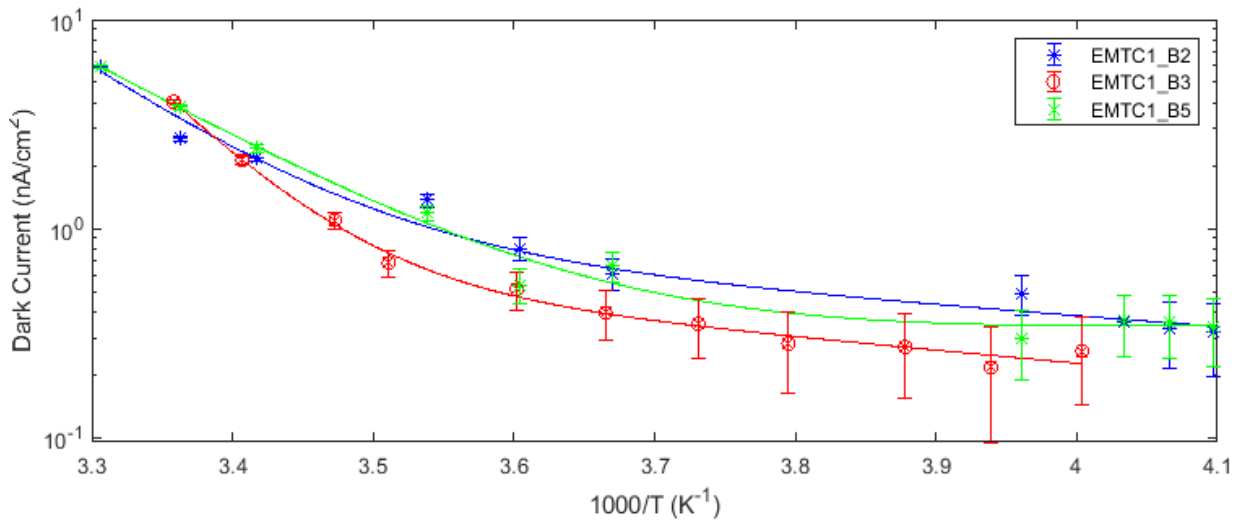


Figure 5: Mean dark current of various EMTC1 image sensors versus reciprocal temperature.

These values can then be compared to dark current values seen in scientific and commercial grade image sensors. Early devices experienced considerably higher dark current (~ 7.0 nA/cm²) [23] than that seen in many modern image sensors which demonstrate dark currents equivalent to the EMTC1 [24] and below [25].

Table 3: The dark current for several regions of the device at 293 K. These dark currents have been averaged over four different EMTC1 image sensors.

Device	Dark Current (nA/cm ²)
EMTC1_B2	2.04±0.58
EMTC1_B3	1.42±0.39
EMTC1_B5	1.45±0.35

Charge Transfer Inefficiency

The charge transfer inefficiency of the EMTC1 was measured using the Extended Pixel Edge Response (EPER) method [19]. Flat-fields images were taken with increasing illumination using an LED and the deferred charge was measured in the overscan region over 100 images using the same integration time (~100 ms).

The CTI was then calculated by using

$$CTI = \frac{S_D}{S_{LC} \cdot N_p} \quad (1)$$

Where S_D is the total deferred charge (electrons) in the extended pixel region, S_{LC} is the charge in the last column (electrons) and N_p is the total number of transfers. The CTI was acquired at 250 K and the difference between each block can be seen in Figure 6. The CTI does vary across the different blocks however, the trend is largely uniform across the device. It is apparent that at both low and high input signal the CTI is higher. Figure 6 demonstrates that Block 5 experiences the lowest CTI, corroborating the expected decrease in trapped charge seen in simulated data for larger gate lengths.

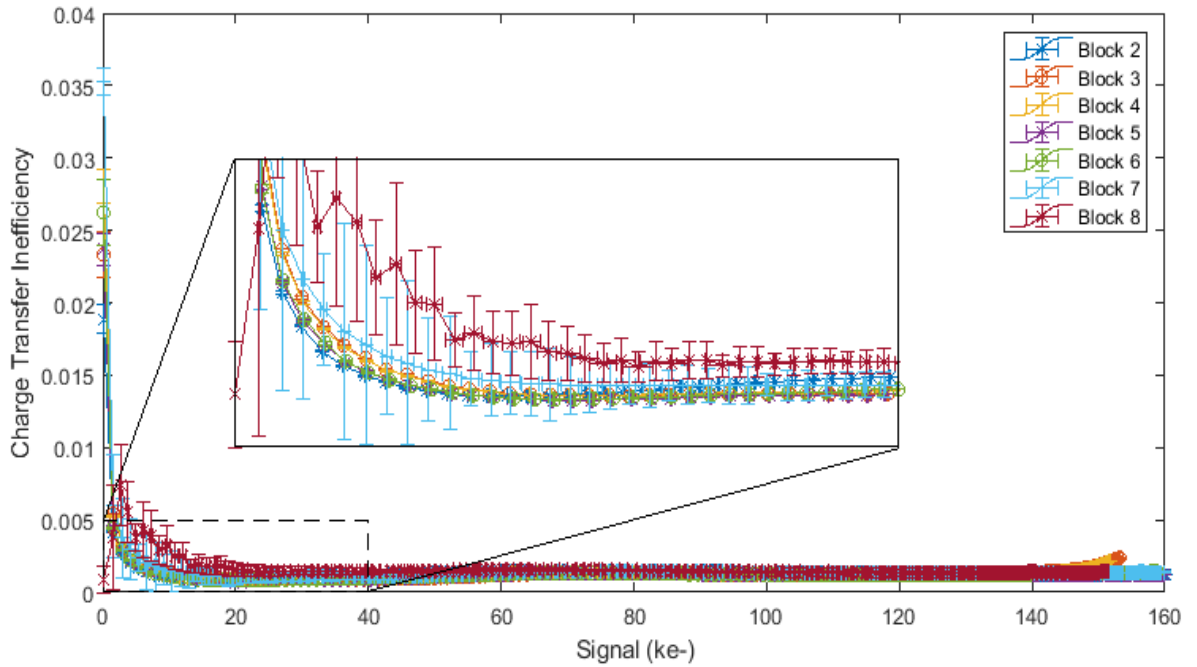


Figure 6: The charge transfer inefficiency calculated from the EPER method at 250 K. The device was illuminated using a uniform light source.

For the EMTC1 to achieve a sufficient electric field to induce impact ionisation and subsequently EM gain, the device requires a P2HV voltage exceeding 10.0 V. It is possible to analyse the effect of the P2HV gate on the CTI by operating

the device at a voltage less than 10.0 V. Figure 7 demonstrates the CTI as the P2HV voltage was increased from 4.0 V to 8.0 V at 283 K for Block 6. It is apparent that as the P2HV voltage increases the CTI also increases.

When operating at higher P2HV gate voltages, it is possible that a proportion of the charge can be trapped during each transfer. If this emission trap time is small, then the charge is re-emitted directly into the same packet, and no impact on the CTI can be detected. If the emission trap time is longer, trapped charge packets can be released during subsequent transfers and entering new charge packets and be registered as signal passing through the EM register.

If the emission time is longer it is possible for an increase in the CTI to be registered, as demonstrated in Figure 7. As the P2HV voltage increases, the CTI rises because the charge moves closer to the surface leading to a greater probability of interaction with the interface. However as the P2HV increases the EM gain also increases counteracting the losses due to CTI.

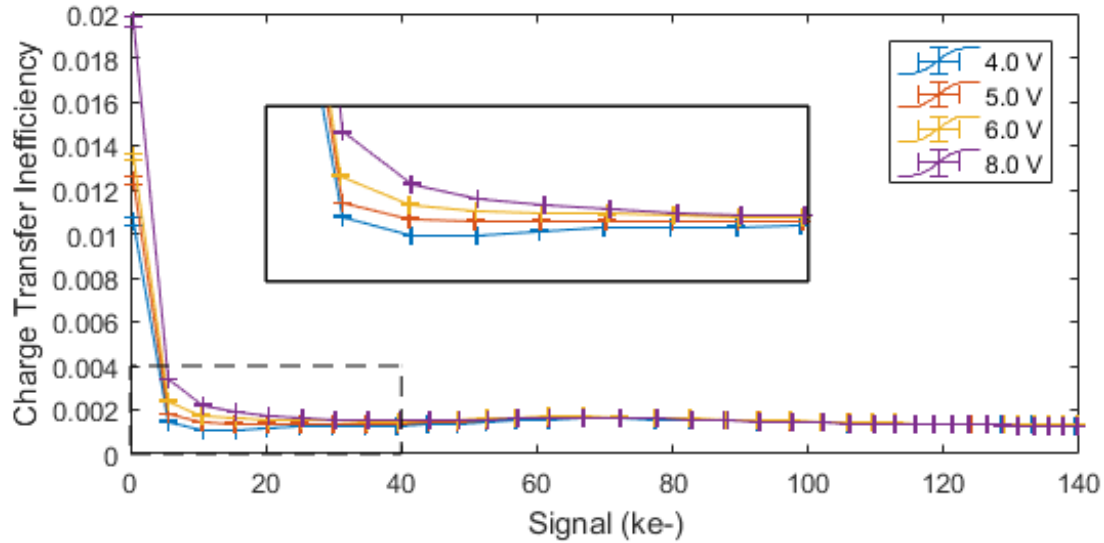


Figure 7: The Charge Transfer Inefficiency for block 6 at 253 K. The device normally achieves gain greater than unity at P2HV voltages greater than 10.0 V. The voltage was increased at increments of 2.0 V from 4.0 V to 8.0 V.

6. THE FUTURE OF THE EMTC1

EMCCDs have been developed with the aim of being implemented in low light environments. A number of space missions have been planned utilising EMCCDs to image in a range of wavelengths including X-ray [26] and visible light [27]. The devices utilised in these missions often require P2HV voltages to be in the range of 40 – 50 V. The high voltages required can prove problematic in restricted power missions. The EMTC1 provides the opportunity to offer an equivalent multiplication gain at much lower voltages in the range of 12 – 15 V. Furthermore, the two new pixel structures are able to reach a gain far exceeding that seen in many commercial and scientific EMCCD devices. These devices have also demonstrated a comparable dark current but a higher CTI than other modern devices.

Future iterations of the EMTC1, which will likely focus on one pixel structure will require extensive analysis to ensure that the correct voltage is used maximising the EM gain limit any saturation which would potentially lead to EM ageing and reduce the CTI. Furthermore, the tolerance to radiation damage and greater resistance to ageing have demonstrated that the EMTC1 provides steps towards an image sensor that could be used in a range of fields including biomedical imaging, industrial applications and space imaging.

7. CONCLUSIONS

The EMTC1 is a novel test chip that has provided an increased understanding of electron multiplication in a CMOS process. Simulation of several EMCCD pixels which vary in length has provided insight into the movement of the charged particle and the primary regions of impact ionisation occurring within an EMCCD in a CMOS process and the effect of length of the gate.

The EMTC1 provides a unique insight into the operation of an EMC MOS device to offer a superior gain per stage at a much lower voltage. The potential for this device in space missions has yet to be fully understood, however, early research demonstrates that future versions could provide a suitable alternative to many modern scientific EMCCDs.

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